

WHAT IS CLAIMED IS:

- 1 1. A method for manufacturing ROM memory devices, the method
2 comprising:
 - 3 forming a trench isolation structure within a cell region of a semiconductor
4 substrate, the cell region being an array region for ROM memory devices;
 - 5 forming a gate structure within the cell region;
 - 6 forming a sidewall spacer on the gate structure, the sidewall spacer structure
7 being configured to overlap a portion of the trench isolation structure within the cell region to
8 separate a buried bit line region of the cell region from an adjacent cell region;
 - 9 applying a refractory metal layer overlying the gate structure including
10 sidewall spacers and exposed portion of the trench isolation structure;
 - 11 alloying the refractory metal layer to the gate structure and exposed portions
12 of source/drain regions to form silicided regions overlying the gate structure and source/drain
13 regions; and
 - 14 selectively removing the refractory metal layer from sidewall spacers and
15 exposed portion of the trench isolation structure.
- 1 2. The method of claim 1 wherein the refractory metal layer is titanium or
2 cobalt.
- 1 3. The method of claim 1 wherein the trench isolation region is an STI
2 region.
- 1 4. The method of claim 3 wherein the STI region comprises silicon
2 dioxide.
- 1 5. The method of claim 1 wherein the cell region has a channel region
2 using a length of about 0.25 micron and less.
- 1 6. The method of claim 1 wherein the sidewall spacer is a dielectric
2 material.
- 1 7. The method of claim 1 wherein the buried bit line structure is within
2 the source/drain region.

1 8. The method of claim 1 wherein the trench isolation is within the
2 semiconductor substrate at a predetermined depth, the predetermined depth being greater than
3 a junction depth of the buried bit line.

1 9. The method of claim 1 wherein the gate structure has a width of 0.25
2 micron and less.

1 10. The method of claim 1 wherein the array has at least eight cells by
2 eight cells.

1 11 A semiconductor integrated circuit memory device structure
2 comprising:
3 a semiconductor substrate, the semiconductor substrate including a memory
4 cell array region for ROM devices and a peripheral region; each of the memory cells
5 including:

6 a trench isolation structure within the memory cell region;
7 a gate structure within the memory cell region;
8 a source/drain region adjacent to the gate structure;
9 a channel region adjacent to the source/drain region and underlying the
10 gate structure;

11 a buried bit line region coupled to the source/drain region and the
12 channel region;

13 a sidewall spacer on the gate structure, the sidewall spacer structure
14 being configured to overlap a portion of the trench isolation structure within the
15 memory cell region to separate the buried bit line region of the memory cell region
16 from an adjacent memory cell region and being configured to overlap a portion of the
17 source/drain region;

18 a refractory metal layer formed overlying a top portion of the gate
19 structure and an exposed portion of the source/drain region while maintaining the
20 sidewall spacer and exposed portion of the trench region structure free from the
21 refractory metal layer.

1 12. The device of claim 11 wherein the buried bit line region is an
2 implanted .region.

1 13. The device of claim 11 wherein the peripheral region comprises one or
2 more MOS transistor structures.

1 14. The device of claim 11 wherein the refractory metal layer is a titanium
2 silicide layer.

1 15. The device of claim 11 wherein the channel region has a length of
2 about 0.35 micron and less.

1 16. The device of claim 11 wherein the trench isolation structure is formed
2 to a predetermined depth, the predetermined depth being greater than a junction depth of the
3 buried bit line region.

1 17. The device of claim 11 wherein the exposed portion of the trench
2 region and the sidewall spacer portion that overlaps the portion of the trench isolation region
3 separates the buried bit line region of the memory cell from the adjacent memory cell region.

1 18. The device of claim 11 wherein the source/drain region is within the
2 buried region.

1 19. The device of claim 11 wherein the gate structure is an MOS transistor
2 gate structure.

1 20. A ROM semiconductor device comprising:
2 a plurality of alternatively arranged select lines and bit lines defined on a
3 silicon substrate;

4 a plurality of word lines arranged substantially orthogonal to the select lines
5 and the bit lines defined on the silicon substrate;

6 a plurality of isolation blocks defined in etched trench regions of the silicon
7 substrate, each of the blocks being formed between a mutually orthogonal pair of word lines
8 and bit lines or select lines to isolate the mutually orthogonal pair of word lines and isolate
9 the bit lines or isolate the select lines.

1 21. The ROM device of claim 20 further comprising one or more MOS
2 transistor structures on a peripheral region outside of the plurality of word lines, select lines,
3 and bit lines.

1 22. The ROM device of claim 20 wherein the select lines and the bit lines
2 are heavily doped regions in the silicon substrate.

1 23. The ROM device of claim 20 wherein each of the word lines comprise
2 sidewall spacers defined on edges of the word lines, each of the sidewall spacers include a
3 portion that overlaps a portion of a plurality of isolation blocks and overlaps a portion of bit
4 lines.

1 24. The ROM device of claim 20 wherein the isolation blocks are formed
2 in the silicon substrate to a predetermined depth, the predetermined depth being greater than a
3 junction depth of the bit lines.

1 25. The ROM device of claim 20 further comprising a refractory metal
2 layer formed overlying exposed portions of the bit lines and select lines and formed overlying
3 exposed portions of the

1 26. The ROM device of claim 25 further comprising a pair of sidewall
2 spacer structures defined on each of the word lines, the sidewall spacer structure being free
3 from the refractory metal layer.